PROFILE

1. NAME AND DESIGNATION : Mr DINEEP S

Assistant Professor

Department of Aeronautical Engineering

S.J.C. Institute of Technology, P.B.

20, B B Road,

Chickballapur-562101, Karnataka

Email: **dineepadharsh@gmail.com**

2. DATE OF BIRTH : 25-11-2001

3. RESIDENTIAL ADDRESS : Vinayaka nagar, gauribidanur ,Chikkballapur , KARNATAKA -561206, India

4. EDUCATIONALQUALIFICATION:

Degree	**Year**	**Specialization**	**Institution / University**
M.E	2026	Power Electronics	RV College of Engineering
B. E	2024	Electronics and Communication Engineering	BMS College of Engineering

5. INTERNSHIP

Intern – RF and Analog System Design (Antenna Design) at B M S College of Engineering

- Designed a transparent antenna system for 5G applications
- Performed simulation and performance analysis using HFSS
- Gained exposure to high-frequency analog behavior and optimization

POWERTRONIX SYSTEMS LIMITED

- Designed and simulated a 2 kVA single-phase inverter using MATLAB/Simulink
- Developed and analyzed solar PV system designs
- Performed inverter testing and system performance evaluation

6. PROJECTS

Digital Twin Based Controller for a Bi-Directional DC-DC Converter Feb 2026-May 2026

Designed and simulated a Digital Twin-based Bi-Directional DC-DC Converter using MATLAB/Simulink and VS Code.

• Developed control algorithms for bidirectional power flow, battery charging/discharging, and regenerative braking.

• Implemented a real-time Digital Twin framework to monitor voltage, current, temperature, power flow, and battery SOC.

RTL to GDSII Implementation and Optimization of a 16-Bit Hybrid Adder Jan 2025-Mar 2025

Designed and optimized a 16-bit hybrid adder using RTL-to-GDSII flow in Cadence tools

• Achieved timing closure with optimized power and area

• Performed STA, DRC, LVS, and LEC verification

• Gained exposure to layout-aware design and manufacturability considerations

Fault Detection in 9 Level-Multilevel Inverter Dec 2025-Feb 2026

Designed and simulated a nine-level multilevel inverter using MATLAB/Simulink

• Implemented voltage- and current-based open-switch and short-circuit fault detection

• Analyzed RMS voltage, current, and total harmonic distortion under fault conditions

• Relevant to power IC reliability, fault tolerance, and power management systems

Error-Correcting Code (ECC) Memory Design using Verilog May 2025-Aug2025

Designed and verified ECC memory using Hamming SEC-DED technique

• Achieved single-bit error correction and double-bit error detection

Design and Implementation of FIR Filters for Noise Cancellation using MATLAB, Verilog HDL, DSK Processor Simulation Nov 2022-Jan 2023

Designed FIR filters for digital noise cancellation using MATLAB and Verilog HDL

• Analyzed spectral characteristics of signals to reduce noise during transmission and reception

• Validated filter performance using DSK processor simulation

Eye Controlled Wheel Chair Monitoring System Feb 2024-May 2024

The Developed a real-time eye-tracking–based wheelchair control system using Raspberry Pi and OpenCV

• Implemented image processing algorithms to translate eye movements into control commands

• Designed a cost-effective assistive solution to improve mobility and independence for users with motor impairments

Digital Moisture Meter Oct 2021-Jan 2022

Designed an IoT-based digital moisture monitoring system using NodeMCU (ESP8266)

• Measured and displayed soil moisture, temperature, and humidity using sensors and digital display

• Enabled wireless data monitoring for applications in agriculture, food storage, and transport

Transparent Antenna System For 5G Applications **Aug 2023-Nov 2023**

Designed a transparent antenna using conductive materials such as ITO/graphene on glass or plastic substrates

• Simulated and analyzed antenna performance for 5G communication applications

• Targeted integration in windows, displays, and wearable devices where conventional antennas are impractical

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7. CERTIFICATIONS

- Verilog HDL; VLSI Hardware Design Comprehensive masterclass course competion by Udemy
- The event Robo Arcade conducted during the International Level Annual
- Technical Symposium sponsored by VIMAAN, Phase Shift 2022, held at BMSCE
- FPGA & SMART GRID COMPATABILITY workshop

8. SKILLS

- **Programming:** C Programming, Verilog HDL, System Verilog, SQL, Basics of Python.
- **Tools:** Cadence Virtuoso, Xilinx Vivado, MAT LAB, LT Spice, HFSS, VS Code, Prime Time, Tempus.
- **Technical:** Digital IC Design, STA, Physical Design, Digital Electronics, Design and Fabrication process, communication protocols (CAN, I2C, UART, USB, Ethernet, LIN).

9. AREAS OF INTEREST:

- *Digital electronics*
- *FPGA*
- *VLSI*
- *Communication Protocols*
- *Verilog HDL*
- *System Veriloge*
- *C programming*
- *Converters*
- *MATLAB*
- *LT Spice*

Date:.28-07-2026

Place: Chickballapur (**Dineep S)**